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Multi-Stacked Flip Chips with Copper Plated Through Silicon Vias for 3D System-in-Package Integration

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Abstract

In the past decade, compact components such as chip scale packages and flip chips are commonly used in many microelectronics products for miniaturization. However, emerging applications require an even higher density of packaging. In order to fulfill this requirement, three dimensional packaging has to be implemented. 3D integrated systems can reduce chip areas and optimize component partitioning. In addition, three dimensional packaging (3DP) structure may lead to minimal conductor length and eliminate speed-limiting inter-chip interconnects. In the microelectronics industry, there are various know-hows for implementing 3DP structures. One of the major technologies is microvias for vertical interconnection. In the past, microvias were mainly made on printed circuit boards or substrates. More recently, the emerging trend is to fabricate through silicon vias (TSVs) on wafers for stacked die applications. In the past few years, some efforts have been made in this area. In general, the forming of TSVs is not a major issue as long as the deep reactive ion etching (DRIE) facility is available. People are able to make TSVs with a diameter less than 5 microns. However, the aspect ratio of microvias is still a concern. Usually substantial wafer thinning is required in order to make through hole microvias. Also, the plugging of microvias is a rather difficult task. People usually use sputtering and plating of copper to fill the TSVs. However, due to the small size of microvias, it is quite difficult to get good quality filling of TSVs. The process development for 3DP remains a challenging area. In this presentation, a new configuration is introduced for the 3D packaging of stacked flip chips. The proposed through holes on wafer are rectangular through silicon slots instead of the conventional round hole vias. The through silicon slots are formed by DRIE. These through silicon slots are distributed along the periphery of chips and go across the saw street between adjacent chips. The through silicon slots are plugged by copper plating. Furthermore, a wafer level re-distribution process is performed to connect the chip I/Os to the through silicon slots and to route I/Os from the through silicon slots to new locations for solder bumping and chip interconnection, which are required for the subsequent 3D die stacking assembly. After the re-distribution and solder bumping processes, the wafer is diced and each chip has half of the original through silicon slots as through hole interconnects along its periphery. Afterwards, these chips can be stacked up to form modules with a 3DP structure. In addition to the design, prototypes have been fabricated during the present study. The package structure and the fabrication processes will be illustrated in details in this presentation. Cross-sectioning and SEM micrographs will be presented as well to demonstrate the features of the proposed 3D stacked flip chip packaging.

Brief Biography

Ricky Lee received his PhD degree from Purdue University in 1992. Currently he is Associate Professor of Mechanical Engineering and Director of Electronic Packaging Laboratory (EPACK Lab) at the Hong Kong University of Science & Technology (HKUST). He is also appointed Chief Technology Officer of Nano and Advanced Materials Institute (NAMI). His research activities cover wafer bumping and flip chip assembly, wafer level and chip scale packaging, microvias and high density interconnects, lead-free soldering and solder joint reliability, and mechanics for sensors and actuators. Ricky has substantial publications in international journals and conference proceedings. He also owns one US patent and co-authored three books. Ricky is a two-time recipient of JEP Best Paper Award (2000 & 2001) conferred by *ASME Transactions: Journal of Electronic Packaging*. He also won the Best Poster Paper Award of IEEE Electronic Components & Technology Conference (ECTC2004) and the Philips Best Paper Award of International Conference on Electronic Packaging Technologies (ICEPT2005). Furthermore, he serves as Editor-in-Chief for *IEEE Transactions on Components & Packaging Technologies* and Associate Editor for *IEEE Transactions on Advanced Packaging*. He also sits on the Editorial Advisory Board of two other international journals. Ricky is very active in professional societies and international conferences. He is an ASME Fellow, an IoP Fellow, and a Senior Member of IEEE. He was Chair of IEEE CPMT-Hong Kong Chapter (2001-2002), Member-at-large of Board of Governors (2003) and Vice-President of IEEE CPMT Society (2004-2005). In addition, he was General Co-Chair of 2nd International Symposium on Electronic Materials and Packaging (EMAP2000) and 60th Chinese Association for Science & Technology Forum for Young Scientists (FYS2001). Currently Ricky is Chair of ASME-Hong Kong Section and Chair of ASME Electronic & Photonic Packaging Division (EPPD). He will serve as General Chair of 8th International Conference on Electronic Materials and Packaging (EMAP2006).